**Ashok Vaddepally**

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*Electrical Engineer looking to be a part of your esteemed organization as a Linux Kernel Developer and aid in organizational growth owing to my skills in Linux, C, HTTP, SMTP, DHCP and JTAG.*

**SUMMARY:**

* Experience in Linux embedded systems development, Linux OS internals
* Experience in C programming language for real time operating systems
* Experience with real time schedulers, multi-threaded programming and inter-process communications in Linux OS environment.
* Experience in developing Peripheral drivers for a Microcontroller using C
* Knowledge in WiFi/Networking protocol implementation and development.
* Hands on Experience in RTL coding, Test bench development and debugging the design.

• Experience with Agile Software development methods, Scrum

**WORK EXPERIENCE:**

**Graduate Assistant at Minnesota State University, Mankato Aug’2015 - May’2017**

* Developed test plan for verifying the 64K X 8 RAM model.
* Monitor, Scoreboard, Generator, Interface components was developed for RAM design

using SystemVerilog

* Verified the functionality of Ethernet on 2x2 router switch and RAM design using UVM.
* Analyzed test results and performed coverage analysis, debugging RTL Codes.
* Developed constraints and cover points for test cases to achieve 100% Functional Coverage.

**Environment:** QuestaSim, GVim Editor, Synopsys VCS, Quartus-II

**Certification in VLSI Design, Center for Development of Advanced Computing, R&D India Aug’2012 - June’2015**

* Case Studied the protocols AMBA -AXI, AHB, APB, Ethernet, I2C.
* Implementation of I2C protocol on FPGA DE0 Board from Altera using Verilog.
* AMBA -AXI, AHB, APB protocols was analyzed and developed verification plan, test cases for them.
* Generated scripts using Tcl to automate the simulation and waveform generation steps for CPU core design.

**Environment:** UNIX, QuestaSim, Synopsys VCS, C, Shell/Perl Scripting, Quartus-II, Xilinx ISE

**TECHNICAL SKILLS:**

**OS :** UNIX/Linux, Windows

**Programming Languages:** C, C++

**HDL/HVL :** VHDL, Verilog, SystemVerilog

**Scripting** : Shell, Tcl, Perl

**Protocols :** AMBA (AXI, AHB, APB), I2C

**FPGA :** Xilinx, Altera

**Simulation Tools :** Modelsim/QuestaSim, Synopsys VCS

CERTIFICATIONS**:**

* Certified Advanced Digital Design in Verilog, **Dec 2015, LucidVlsi, India**
* Certified in SoC Verification using SystemVerilog, **Jan 2017, LucidVlsi, India**

**PUBLICATION:** “TPG Applications Using LFSR” -Fifth International Conference on Advances in Recent Technologies in communication and Computing- Artcom’13**. ISBN: 978-81-910691-8-3.**

**PROJECTS HANDLED**:

# Ethernet packet on 2x2 Router switch design and verification using UVM

**Description:** Analyzed the Ethernet framework and a 2x2 Router switch is designed with user specific requirements and a packet is generated and processed through the Router. Developed Sequencer, Driver, Monitors and Subscriber components. The router accepts packets on a dual 8-bit port called data and routes the packets to one of the two output channels. The test cases are written and verified by writing the constraints to detect the CRC, data channel length errors and dropping of error packets. It can be used as a self-checking test bench environment for the 2x2 Router.

**Tools:** Synopsys VCS, EDA playground, Tcl

# Synchronous RAM slave design and verification model using SystemVerilog and UVM

**Description:** Developed RTL coding for memory model (DUT) and written the verification plan by analyzing different scenarios for testing the memory. complete verification environment and components - generator, driver, monitors, scoreboard are developed from the scratch in SystemVerilog and achieved 100% functional coverage using constrained random stimulus generation. The verification environment is also developed from scratch in UVM. Configuration of the stimulus is achieved by using RAL methodology in UVM.

**Tools:** Synopsys VCS, EDA playground, Tcl

**AMBA AXI VIP Development using SystemVerilog**

**Description:** In this Project, the architecture of AMBA- AXI 3.0 protocol is analyzed and developed the components – driver, generator, Monitor using SystemVerilog and implemented the Coverage. AXI master and slave modules are used to validate the protocol model.

**Tools**: QuestaSim, GVim Editor

# Development of AMBA – APB protocol using SystemVerilog

**Description:** In this project, the AMBA-3 APB protocol v1.0 specification is case studied and developed a verification environment by taking a master and a slave. WAIT states are also installed to check the behavior of APB bus protocol. Developed the DUT driver, Scoreboard, interface, monitor blocks and implemented the test cases. Validated the APB VIP using a APB slave model.

**Tools:** Synopsys VCS, EDA playground

# Implementation of I2C protocol using Verilog

**Description:** Understood the physical connections, Start and Stop conditions, Acknowledgement and Data Transfer by using Virtual master to communicate with the slave, designed system block diagram for Slave. Designed Clock generators, Shift-registers, Slave controller, Counters, Detectors using Verilog.

**Tools**: Quartus-II, Vim Editor, Altera DE0 Board

**EDUCATION**:

Master of Science in Electrical Engineering, Minnesota State University, Mankato - May’2017 GPA: 3.46/4

Bachelor of Technology in Electronics Engineering, Kakatiya University – May'2013 GPA:3.5/4